UNIVERSITÉ LIBRE DE BRUXELLES

Prof. Dragomir MILOJEVIC

Curriculum Vitae

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Short CV

Dragomir Milojevic received his master's and PhD degrees in Electrical Engineering from Ecole Polytechnique de Bruxelles (EPB), Université libre de Bruxelles (ULB), Belgium. Between 1999 and 2006 he worked at ULB as a teaching assistant in the field of digital logic circuits. In 2005 he joined IMEC where he first worked on multi-processor and Network-on-Chip architectures for low-power multimedia systems. Since 2008 he is working on design enablement and characterization of advanced CMOS technologies (<10nm) & 3D stacked integrated circuits. Today, part of INSITE & 3D integration programs at IMEC, he is working on system architecture and design technology co-optimization. Since 2006, Dragomir Milojevic holds the position of a professor at EPB, where he co-founded Parallel Architectures for Real-Time Systems (PARTS) multi-disciplinary research group.

Education

Active courses

- Logic circuits (ELEC-H-305, ULB)
- Multidisciplinary project (ELEC-H-309, ULB)
- Digital electronics (ELEC-H-310, 5 ECTS, ULB)
- Digital architectures & design (ELEC-H-409, 4 ECTS, BRUFACE ULB - VUB)
- Project in telecommuncation (ELEC-H-415, BRUFACE ULB - VUB)
- Microprocessor architectures (ELEC-H-473, 5 ECTS, BRUFACE ULB - VUB)
- Advanced Digital Architecture (ELEC-H-505, 5 ECTS, BRUFACE ULB - VUB)
- Programmable Logic Controllers (ELEC-H-516, 3 ECTS, ULB)

Management responsibilities

- 2018 - today: President of Electronics & Telecommunication council, ULB
- 2018 - today: Co-President of Electrical Engineering educational council, BRUFACE (ULB-VUB)
- 2008 – today: Co-President of PARTS research group (3 academics & 10 researchers)
- 2012 - today: Responsible for student mobility (Electronics & Telecommunication)
- 2012 - 2018: Academic responsible for admissions to BRUFACE program

Scientific profile

Author or co-author of more than 150 publications in peer-reviewed journals and conference proceedings. Co-author of a book and three book chapters. Google scholar: 821 citations, h-index of 15, i10-index of 24

Five main publications

Book chapter and most recent articles on 3D system integration:

[1] **Milojevic, D.**, Agrawal, P., Raghavan, P., Plas, G. V. D., Catthoor, F., & Beyne, E. (2019). Handbook of 3D Integration: Ultra-Fine Pitch 3D-Stacked Integrated Circuits: Technology, Design. DOI: https://doi.org/10.1002/9783527697052.ch2

[2] **D. Milojevic**, G. Sisto, G. Van der Plas, E. Beyne, "Fine-pitch 3D system integration and advanced CMOS nodes: technology and system design perspective," Proc. SPIE 11614, Design-Process-Technology Co-optimization, https://doi.org/10.1117/12.2584532, 2021

[3] R. Chen, P. Weckx, S. M. Salahuddin, S.-W. Kim, G. Sisto, G. Van der Plas, M. Stucchi, R. Baert, P. Debacker, M. Na, J. Ryckaert, **D. Milojevic**, and E. Beyne. 3D-optimized SRAM Macro Design and Application to Memory-on-Logic 3D-IC at Advanced Nodes. In 2020 IEEE International Electron Devices Meeting (IEDM), pages 15.2.1–15.2.4, 2020

[4] G. Sisto, P. Debacker, R. Chen, G. Van der Plas, E. Beyne, R. Chou, and **D. Milojevic**. Design enablement of fine pitch face-to-face 3D system integration using die-by-die place & route. In IEEE 2019 International 3D Systems Integration Conference, 2019.

Recent collaborative work with Georgia Tech, University of Bremen and IMEC on 3D-IC:

[5] L. Zhu, L. Bamberg, S. Pentapati, K. Chang, F. Catthoor, **D. Milojevic**, M. Komalan, B. Cline, S. Sinha, X. Xu, A. Garcia-Ortiz, and S. K. Lim, "High-Performance Logic-on-Memory Monolithic 3D IC Designs for Arm Cortex-A Processors," IEEE Transactions on Very Large Scale Integration Systems, in-print, 2021.

Other scientific output and impact (only mention most relevant)

Ph.D. supervision

- Supervisor of 6 Ph.D. students (2 defended, 4 ongoing)
- Co-supervisor of 5 Ph.D. students (5 defended)
- Co-supervisor of 1 postdoc

Valorization experience and industrial collaboration

Research funding

- 1 ARC (Action de Recherche Concertée) grant: SOFIST (2016-2020), principal instigator
- 5 EU findings (CRAFTERS (2012-2015) co-instigator; co-instigator for the following EU H2020 projects: Eurocloud, Therminator, ParaDime)
- Ph.D. fellowships: 1 FRIA, 1 China Scholarship Council, 1 industrial (Cadence DA, USA)
- Brussels/Wallonia projects: 1 Spin-off PAPARETO (2012-2015)

Active collaborations

- 2005 - today: IMEC, principal scientist
- 2015 - today: Georgia Tech, School of Electrical and Computer Engineering, Prof. Sung-Kyu Lim
- 2007 - today: LIP6, Université de Sorbonne (UPMC) Prof. Bertrand Granado

Spin-off companies

- Co-founder of two companies: VISAR (2000) & HIPPEROS (2015)